2014-1509

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS,

Appellant,

v.

MICRON TECHNOLOGY, INC.,

Appellee.

Appeal from the United States Patent and Trademark Office before the Patent Trial and Appeal Board in case no. IPR2013-00005, Administrative Patent Judges Sally Gardner Lane, Bryan F. Moore, and Michael J. Fitzpatrick

BRIEF OF APPELLANT THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS

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July 29, 2014

CERTIFICATE OF INTEREST

Pursuant to Fed. Cir. R. 47.4, counsel for appellant, The Board of Trustees of the University of Illinois, certifies the following:

(1) The full name of every party or amicus represented by me is: The Board of Trustees of the University of Illinois.

(2) The name of the real party in interest represented by me is: The Board of Trustees of the University of Illinois.

(3) All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are: None.

(4) The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

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STATEMENT OF RELATED CASES

There are two companion appeals to the instant appeal, Appeal Nos. 2014-1510 and 2014-1511.

JURISDICTIONAL STATEMENT

This Court's jurisdiction over this appeal is governed by 28 U.S.C. § 1295(a)(4)(A).

STATEMENT OF THE ISSUE

Whether the Board erred in finding that the limitation from claims 2 and 3 of U.S. Patent No. 6,444,533 ("the '533 Patent") "by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime" is necessarily found in WO94/19829 to Lisenker, *et al.* ("Lisenker"), such that this limitation is inherent in that reference.

STATEMENT OF THE CASE

On December 5, 2011, Appellant, The Board of Trustees of The University of Illinois ("the University") filed suit for patent infringement in the United States District Court for the Central District of Illinois asserting three patents, including the '533 Patent against Appellee, Micron, Inc. ("Micron"). On October 2, 2012, Micron filed a petition for *inter partes* review of the '533 Patent. On March 10, 2014, the Board issued a final determination canceling claims 1-8 of the '533 Patent, given their obviousness in light of, *inter alia*, Lisenker.[1]

[1] The University only appeals from the final determination pertaining to claim 2 and 3 of the '533 Patent.

STATEMENT OF FACTS

The '533 Patent solves a problem known as "hot carrier effects" at the interface of the silicon and insulator layers of a semiconductor device. Hot carrier effects in a semiconductor device occur when channel carriers become sufficiently energetic and enter the insulator layer, which degrades the device. (A94, column 1, lines 61-67.) The '533 Patent discloses results comparing wafer samples annealed in a deuterium ambient with wafer samples annealed in a hydrogen-based ambient, demonstrating that "transistors sintered in deuterium typically exhibit lifetimes 10 times longer than those sintered in hydrogen." (A97, column 8, lines 39-47.)

Claim 2 of the '533 Patent explicitly requires this 10-fold increase in device lifetime:

> A process for treating an insulated gate field effect transistor device structure including a channel region extending between source and drain regions, a gate insulating layer having an interface with said channel region, and contacts to said source and drain regions and on said gate insulator layer, comprising forming said gate insulator beneath the gate contact to have a thickness not greater than about 55 Angstroms and, subsequent to formation of said source, drain and gate contacts, annealing the device in an ambient including deuterium at a temperature above about 200^{o} C. and below a decomposition or melting temperature of said structure to form a concentration of deuterium at said interface region effective to substantially reduce degradation of said device associated with hot carrier stress ***by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime*** is taken as 20% transconductance degradation as a result of electrical stress.

(A98, column 9, line 4 – column 10, line 2 (emphasis added).)

Claim 3 of the '533 Patent depends from claim 2, and adds the limitation "wherein said temperature is about 400° C." (*Id.*, column 10, lines 3-4.)

In seeking *inter partes* review of the '533 patent, Micron relied heavily upon Lisenker as invalidating prior art. The University urged in response below that the claimed results from post-metallization passivation cannot be inherent in Lisenker, which emphasizes deuterium passivation ***before*** the formation of metal contacts on a semiconductor device, *i.e.*, pre-metallization annealing. (*See* A9-A10.) Specifically, if passivation takes place pre-metallization, "the deposited deuterium migrates away from the interface during subsequent processing." (A13.) Micron's expert below agreed with this proposition. (A189-A190, ¶ 15.)

Further, Micron's expert presented data purporting to replicate Lisenker's work, which reflected an improvement in device lifetime of as little as about three to four fold. (A749-A750, ¶ 23.) The University's expert, for his part, estimated that the improvement in device lifetime resulting from Lisenker was even more modest 1.2 to 2.5 times, which is far below the 10-fold lifetime claimed in '533 Patent. (A630-A631, ¶ 29.)

Despite this evidence, in its final determination canceling the claims of the '533 Patent, the Board ruled that claims 2 and 3 of the '533 Patent are obvious in light of Lisenker in combination with other references. (A20.) Central to the ruling was the Board's finding that Lisenker satisfied the claimed increase in

practical device lifetime. (A15-A16.) The Board tacitly acknowledged that this claimed increase was not expressly taught in Lisenker, but that such increase was nonetheless inherent in Lisenker, the evidence of such inherency apparently being the '533 Patent itself. (A15 ("The italicized portion of the above-quoted limitation is the inherent result of the claimed process, which process also is taught by Lisenker.").) The Board also referenced a single claim from Lisenker "wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 99:1." (A14.)

At the same time, however, the Board acknowledged that "Lisenker is ***not limited*** to pre-metallization deuterium passivation." (A13 (emphasis added).) In other words, Lisenker was at best agnostic as to whether to perform passivation pre- or post-metallization.

SUMMARY OF ARGUMENT

The Board found that Lisenker inherently satisfied the limitation from claims 2 and 3 of the '533 Patent specifying a 10-fold increase in semiconductor device lifetime resulting from post-metallization deuterium annealing. Yet, experimental data reflecting results far below this 10-fold increase presented by ***both*** parties' experts below belie that conclusion. Further, as Lisenker teaches the use of pre- and post-metallization annealing as being effectively interchangeable (indeed Lisenker emphasizes pre-metallization annealing), the results obtained from post-metallization annealing claimed in the '533 Patent cannot be necessarily present when practicing Lisenker. Finally, none of the reference combinations relied upon by the Board solves for the absence in Lisenker of the 10-fold lifetime improvement claimed in the '533 Patent.

STANDARD OF REVIEW

The propriety of a decision of the Board cancelling a patent pursuant to 35 U.S.C. § 103 is a question of law with underlying issues of fact. *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013). This court reviews the Board's compliance with governing legal standards *de novo* and its underlying factual determinations for substantial evidence. *In re Sullivan*, 498 F.3d 1345, 1350 (Fed. Cir. 2007).

ARGUMENT

Inherency requires that a limitation expressly missing from a prior art reference be "necessarily present" in such reference. *Verizon Servs. Corp. v. Cox Fibernet Va., Inc*., 602 F.3d 1325, 1338 (Fed. Cir. 2010) (quoting *Schering Corp. v. Geneva Pharms., Inc*., 339 F.3d 1373, 1377 (Fed. Cir. 2003)); *see also In re Omeprazole Patent Litig*., 483 F.3d 1364, 1378 (Fed. Cir. 2007); *Trintec Indus., Inc. v. Top-U.S.A. Corp*., 295 F.3d 1292, 1295 (Fed. Cir. 2002).

The inherent result must inevitably result from the disclosed steps. "'Inherency . . . may not be established by probabilities or possibilities. The mere fact that a certain thing ***may*** result from a given set of circumstances is not sufficient.'" *Bettcher Indus., Inc. v. Bunzl USA, Inc*., 661 F.3d 629, 639 (Fed. Cir. 2011) (quoting *In re Oelrich*, 666 F.2d 578, 581 (C.C.P.A. 1981)) (emphasis added); *see also Therasense, Inc. v. Becton, Dickinson & Co.*, 593 F.3d 1325, 1332 (Fed. Cir. 2010); *Cont'l Can Co. USA v. Monsanto Co*., 948 F.2d 1264, 1269 (Fed. Cir. 1991).

As explained in detail in the University's Statement of Facts, given the technical analyses of the parties' respective experts reflecting lifetime improvements of as little as 1.2 to 3 fold, there is a serious question as to whether one practicing Lisenker ***ever*** (let alone inevitably) would obtain the 10-fold lifetime improvement claimed in the '533 Patent. Further, as Lisenker's teachings

are not limited to post-metallization annealing, and given that results differ fundamentally when annealing occurs pre- versus post-metallization, the results obtained when practicing Lisenker's teachings are anything but consistent. The 99:1 ratio of deuterium to hydrogen cited by the Board from a single claim in Lisenker does not convert the inconsistent into the consistent.

The purported improvement in Lisenker is a possibility at most. It is certainly not a necessity, as is required for a feature purportedly inherent in the prior art. Thus, the Board erroneously determined that Lisenker inherently yields the claimed improvement, and that determination should be reversed.

As noted above, the Board's apparent "evidence" of the purported inherent lifetime improvement was the '533 Patent itself. However, "[a]n inventor's explanation of how the invention works does not render obvious that which is otherwise unobvious." *In re Glaug*, 283 F.3d 1335, 1341 (Fed. Cir. 2002). According to this Court, the patent's own "teaching that the spacing permits the fabric to bunch and stretch is not evidence of obviousness." *Id.* If anything, that teaching "supports the unobviousness of [the patentee's] discovery." *Id.* Given that its ***only*** evidence of inherency is found in the '533 Patent, the Board's obviousness determination was erroneous.

The Board also made findings regarding the obviousness of claims 2 and 3 of the '533 Patent in light of combinations of prior art references. (A20.)

However, the Board did not rely on any of these combinations to satisfy the increased lifetime limitation from that claim, either by inherency or otherwise.

The Board did rely upon certain prior art combinations to arrive at post-metallization passivation using deuterium. (A17 (Lisenker in view of Ito); A17-A19 (Deal in view of Lisenker).) However, nowhere does the Board explain the motivation to combine these references. And given Lisenker's failure to distinguish between pre- and post-metallization annealing in achieving the reported superior results, there would have been no motivation for one of ordinary skill in the art reading Lisenker to have sought out other references teaching post-metallization annealing specifically.

Finally, there is no evidence that one skilled in the art practicing any of these combinations would have ***necessarily*** obtained the claimed enhanced practical device lifetime. Indeed, as there is no evidence that anyone actually employed any such combination, predicting the results therefrom would be mere speculation.

CONCLUSION AND RELIEF SOUGHT

For the foregoing reasons, the University respectfully requests that the cancellation of claims 2 and 3 of U.S. Patent 6,444,533 be vacated and that the matter be remanded to the Board for further action consistent with such *vacatur*.

Respectfully submitted,

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ADDENDUM

ADDENDUM

Trials@uspto.gov
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Paper No. 54
March 10, 2014

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.
Petitioner

v.

THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS
Patent Owner

Case IPR2013-00005
Patent 6,444,533 B1

Before SALLY GARDNER LANE, BRYAN F. MOORE, and MICHAEL J. FITZPATRICK, *Administrative Patent Judges*.

FITZPATRICK, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
35 U.S.C. § 318 and 37 C.F.R. § 42.73

BACKGROUND

Micron Technology, Inc. ("Micron") filed a Petition (Paper 3, "Pet.") requesting an *inter partes* review of all claims (i.e., claims 1-8) of U.S. Patent No. 6,444,533 B1 (the "'533 patent"). The Board of Trustees of the University of Illinois ("University") filed a Patent Owner Preliminary Response (Paper 14, "Prelim. Resp."). In a March 13, 2013, Decision to Institute (Paper 19, "Dec. on Pet."), the Board granted the Petition and instituted trial of all claims on the following grounds:

claims 1-8 as obvious over Lisenker (Ex. 1006)[1];

claims 1-8 as obvious over Lisenker in view of Ito (Ex. 1005)[2];

claims 1-8 as obvious over Deal (Ex. 1009)[3] in view of Lisenker; and

claims 1-8 as obvious over Deal in view of Lisenker and Ito.

Dec. on Pet. 20.

After institution, the University filed a Patent Owner Response (Paper 26, "PO Resp."). In it, the University opposes the grounds of unpatentability on two general bases: (1) the Board's findings, in instituting trial, regarding Lisenker are incorrect; and (2) objective indicia prove the claims would not have been obvious. Micron filed a Reply (Paper 28). Oral hearing was held on December 9, 2013.[4]

The Board has jurisdiction under 35 U.S.C. § 6(c). This final written Decision, issued pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73, addresses issues and arguments raised during the trial. Issues and arguments

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[1] WO 94/19829 to Lisenker et al. (Sep. 1, 1994).
[2] US 4,980,307 to Ito et al. (Dec. 25, 1990).
[3] US 4,027,380 to Deal et al. (June 7, 1977).
[4] A transcript of the final hearing is included in the record.

raised prior to institution of trial, but not made during trial, are not addressed necessarily in this Decision.

As discussed below, Micron has shown by a preponderance of the evidence that claims 1-8 of the '533 patent are unpatentable.

A. Related Proceedings

Micron indicates that it is a named defendant in a pending district court case concerning the '533 patent brought by the University and captioned *The Board of Trustees of the University of Illinois v. Micron Technology, Inc.*, Case No. 2:11-cv-02288 (C.D. Ill.). Pet. 1.

Also, Micron filed two additional petitions, which we granted, for *inter partes* reviews of two related patents: IPR2013-00006, regarding U.S. Patent No. 6,888,204, and IPR2013-00008, regarding U.S. Patent No. 5,872,387.

B. The '533 Patent (Ex. 1002)

The '533 patent, titled "Semiconductor Devices And Methods For Same," is assigned to the University. Ex. 1002, 1. The '533 patent issued from U.S. Application Serial No. 09/518,802, filed March 3, 2000. *Id.*

The '533 patent "relates to methods for treating semiconductor devices or components thereof in order to reduce the degradation of semiconductor device characteristics over time." Ex. 1002, col. 1, ll. 13-16. In particular, the '533 patent discloses methods of treating a semiconductor device by passivation of (or annealing[5]) the device with deuterium, an isotope of hydrogen. *Id.* at col. 2, ll. 25-28; Prelim. Resp. 1. The '533 patent explains:

[5] Micron's witness testified that passivation is also referred to as annealing. Ex. 1001 (declaration of Michael L. Reed, Ph.D. ("Reed Decl.")) ¶ 14.

> [T]reatment with deuterium provides a reduction in the depassivation or "aging" of semiconductor devices due to hot-carrier effects. Such aging is evidenced, for example, by substantial degradations of threshold voltage, transconductance, or other device characteristics. In accordance with the present invention, semiconductor devices are fabricated using deuterium to condition the devices and stably reduce the extent of these degradations.

Ex. 1002, col. 3, ll. 27-35.

Prior to the '533 patent, passivation with hydrogen[6] was "a well-known and established practice in the fabrication of semiconductor devices" to remove defects that affect the operation of the devices. Ex. 1002, col. 1, ll. 17-21; *see* Ex. 1001 (Reed Decl.) ¶¶ 13-14. According to the '533 patent, it was "discovered that semiconductor devices, for example including MOS[7] devices, can be advantageously treated with deuterium to improve their operational characteristics." Ex. 1002, col. 2, ll. 22-25.

C. Illustrative Claims

Claims 1 and 2 are the only independent claims of the '533 patent. They are illustrative of the claimed subject matter and read as follows:

> 1. A process for treating a semiconductor device including a semiconductor region and an insulating layer having an interface with the semiconductor region and a contact on said insulating layer overlying said interface, comprising the steps of forming said insulating layer with a thickness not exceeding about 55 Angstroms beneath said contact, and of annealing said semiconductor device, subsequent to completion of fabrication

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[6] Our use of the term "hydrogen" and the symbol "H" in this Decision refers to naturally occurring hydrogen, which we understand to be predominantly protium, but may include trace amounts of deuterium.

[7] MOS refers to metal oxide semiconductor. Ex. 1002, col. 1, ll. 34-35; Ex. 1001 ¶ 9.

of said device, in an ambient including deuterium to form a concentration of deuterium at the interface between said semiconductor region and said insulating layer region effective to substantially reduce degradation of said device associated with hot carrier stress.

2. A process for treating an insulated gate field effect transistor device structure including a channel region extending between source and drain regions, a gate insulating layer having an interface with said channel region, and contacts to said source and drain regions and on said gate insulator layer, comprising forming said gate insulator beneath the gate contact to have a thickness not greater than about 55 Angstroms and, subsequent to formation of said source, drain and gate contacts, annealing the device in an ambient including deuterium at a temperature above about 200° C. and below a decomposition or melting temperature of said structure to form a concentration of deuterium at said interface region effective to substantially reduce degradation of said device associated with hot carrier stress by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

ANALYSIS

A. Claim Construction

In an *inter partes* review, "[a] claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears." 37 C.F.R. § 42.100(b). That construction must be consistent with the specification, and the claim language should be read in light of the specification, as it would be interpreted by one of ordinary skill in the art. *In re Suitco Surface, Inc.*, 603 F.3d 1255, 1260 (Fed. Cir. 2010). Thus, we give claim terms their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir.

2007) ("The ordinary and customary meaning is the meaning that the term would have to a person of ordinary skill in the art in question.") (internal quotation marks omitted).

In instituting trial, we gave each claim term its broadest reasonable interpretation, as understood by one of ordinary skill in the art and consistent with the disclosure of the '533 patent, as neither party had argued persuasively that any claim or term should be construed otherwise.[8] For purposes of institution, we found it useful to set forth, expressly, constructions for two claims terms.

First, we construed the term "subsequent to completion of fabrication of said device," appearing in claim 1, to mean after the contacts on the device are formed. This is the broadest reasonable interpretation consistent with the disclosure of the '533 patent. *See* Ex. 1002, col. 4, ll. 41-43 ("subsequent to the fabrication of device 11 (e.g. subsequent to fabricating the gate, source and drain contacts))"; col. 4, ll. 52-53 ("after fabrication is completed (i.e. after the metal contacts are completed)").

Second, we noted the term "above about 200° C. and below a decomposition or melting temperature of said structure," appearing in claim 2, includes temperatures of up to about 1,000° C. *See* Ex. 1002, col. 5, ll. 1-7 ("The annealing process can be conducted . . . preferably at a temperature of at least about 200° C. up to the melting point or decomposition

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[8] Micron generally asserted that the claims should be "treated as product-by-process claims[.]" Pet. 5-6. Each of the claims, however, is explicitly a "process" or "method," and Micron did not provide any basis or reasons for construing them as product-by-process claims. Hence, we rejected Micron's request to treat them as product-by-process claims.

temperature of other components of the device, more preferably in the range of about 200° C. to about 1000° C., and most typically in the range of about 200° C. to about 800° C.").

During trial, neither party argued for different constructions. As such, we adopt our prior constructions.

B. Prior Art References In Trial

1. Lisenker (Ex. 1006)

Lisenker discloses "a method for producing semiconductor devices in which hydrogen-containing bonds in silicon dioxide are replaced with deuterium containing bonds. Specifically Si-H bonds are replaced with Si-D bonds and Si-OH bonds are replaced with Si-OD bonds." Ex. 1006, 5, l. 36 – 6, l. 3. Lisenker further discloses how the method may be carried out, stating:

> a silicon wafer is contacted with a deuterium containing material to form Si-D and Si-OD bonds in a silicon dioxide layer and on a silicon surface at an interface with the silicon dioxide layer. Typical silicon dioxide layers suitable for treatment according to the present invention include isolation oxides, gate oxides, and various other oxide layers commonly used with semiconductor devices. According to the invention, deuterium or a deuterium-containing material is directed onto the device by, for example, annealing in a deuterium containing atmosphere, and/or cleaning with a deuterium compound such as D_2O, D_2SO_4, and DCl. In general, any hydrogen containing material used in VLSI[9] fabrication can be replaced with corresponding deuterium containing material.

Id. at 4, ll. 20-34. Finally, Lisenker discloses the benefits of the method and how those benefits are purportedly obtained, stating:

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[9] VLSI refers to "very large scale integration." Ex. 1011 (THOMAS E. DILLINGER, VLSI ENGINEERING 4 (Prentice Hall, 1988)).

> The stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms with deuterium atoms. The Si-D and Si-OD bonds thus formed provide completed silicon dangling bonds that are less likely to break when exposed to electrical stresses. Therefore, the deuterium containing devices of the present invention have improved stability, quality, and reliability.

Id. at 4, l. 35 – 5, l. 5.

2. Ito (Ex. 1005)

Ito is titled "Process For Producing A Semiconductor Device Having A Silicon Oxynitride Insulative Film." Ito states that "[t]he gate insulation film should have a thickness of from approximately 30 to 3000 angstroms." Ex. 1005, col. 9, ll. 41-43.

3. Deal (Ex. 1009)

Deal is titled "Complementary Insulated Gate Field Effect Transistor Structure And Process For Fabricating The Structure." It discloses much of the subject matter of claims 1-8, including, in particular, post-metal annealing, albeit in hydrogen. Ex. 1009, col. 9, ll. 33-51. Deal does not disclose using deuterium.

C. Claims 1-8 As Obvious Over Lisenker Alone

As discussed below, Micron has shown a prima facie case that the subject matter of claims 1-8 would have been obvious over Lisenker.

1. Claim 1

Lisenker, as discussed above and below, teaches the subject matter of claim 1 except for the step of "forming said insulating layer with a thickness not exceeding about 55 Angstroms beneath said contact."

The Supreme Court has held that the obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). In that regard, we credit the testimony of Micron's witness, Dr. Reed, that, at the time of filing the '533 patent, it would have been apparent to one of ordinary skill in the art to reduce the thickness of the gate insulating film of Lisenker to 55 Angstroms or less, consistent with the general, decades-long trend of device miniaturization in the semiconductor industry. Ex. 1001 ¶ 38.

We also credit Dr. Reed's testimony that, at the time of filing the '533 patent, others already had made gate insulating films having thicknesses of 55 Angstroms or less. Ex. 1001 ¶¶ 39, 43. The combination of familiar elements according to known methods to achieve predictable results, such as reducing the thickness of the gate insulating film of Lisenker to 55 Angstroms or less, would have been obvious. *See KSR*, 550 U.S. at 416.

We further note that the University does not argue, or direct us to evidence, to show criticality of the thickness limitation, such that we might conclude that obviousness has not been shown. *See generally* PO Resp.; *see* Prelim. Resp. 2. Rather, the University's prior art-based arguments are directed exclusively to Lisenker.

The University makes the following three assertions regarding Lisenker: "[o]ne of ordinary skill would have ignored Lisenker"; "[o]ne of ordinary skill would read Lisenker as limited to pre-metallization passivation"; and the limitation "'[s]ubstantially reduce degradation . . .' is

not inherent in Lisenker." PO Resp. 9, 11, 12 (emphasis removed). We disagree with each of these assertions, as discussed below.

a) One Of Ordinary Skill Would Not Have Ignored The Teachings Of Lisenker

The University argues that the fundamental theory underlying Lisenker's teachings is that "the Si-D bond is significantly stronger than the Si-H bond." PO Resp. 9 (providing no citation to Lisenker).[10] But, according to the University, Lisenker erroneously relies on energy values for bonds not at the interface. PO Resp. 9. The University further argues that a person of ordinary skill in the art at the time of the invention would have known that "the energies for Si-D and Si-H bond disassociation *at the silicon surface* are identical or substantially identical." PO Resp. 10 (emphasis added). Therefore, the University reasons, such a person "would have concluded that the teachings of Lisenker were immaterial to the problem facing the inventors of the ['533] patent, *i.e.*, how to solve for hot carrier effects involving bonds at the silicon substrate." PO Resp. 10 (citing *In re Young*, 927 F.2d 588 (Fed. Cir. 1991)).

Contrary to the implication of the University's argument, however, the scope of the prior art is not limited to solutions that are directed to the problem the patentees set out to solve. *KSR*, 550 U.S. at 419 ("In determining whether the subject matter of a patent claim is obvious, neither the particular motivation nor the avowed purpose of the patentee controls. What matters is the objective reach of the claim. If the claim extends to

[10] Lisenker states that "[t]he stability of oxide layers is improved in the present invention because the bond energy of the Si-H and Si-OH bonds is increased by replacing the hydrogen atoms with deuterium atoms." Ex. 1006, 4, l. 35 – 5, l. 1.

what is obvious, it is invalid under § 103."). Additionally, we disagree with the further implication that Lisenker is not concerned with solving for hot carrier effects involving bonds at the silicon surface (or silicon-silicon dioxide interface). *See* Ex. 1006, 4, ll. 2-12 (discussion by Lisenker of problems caused by hot electrons at the silicon-silicon dioxide interface), Fig. 1 (illustrating an improved silicon-silicon dioxide interface in accordance with the Lisenker invention).

Also, the University's reliance on *In re Young* is not persuasive. *Young* does not support the proposition that a prior art reference may be ignored. *Young*, 927 F.2d at 591 ("Even if tending to discredit [the] Carlisle [patent], [the] Knudsen [article] cannot remove Carlisle from the prior art. Patents are part of the literature of the art and are relevant for all they contain."). In *Young*, the court held that, "[w]hen prior art contains apparently conflicting references, the Board must weigh each reference for its power to suggest solutions to an artisan of ordinary skill." *Id.* Here, the University has presented evidence conflicting, allegedly, with Lisenker's underlying theory of operation. But, the University has not provided a reference conflicting with Lisenker's express teaching that "deuterium containing devices of the present invention have improved stability, quality, and reliability." Ex. 1006, 5, ll. 4-5. Accordingly, we are not persuaded that a person of ordinary skill in the art would have ignored Lisenker.

b) Lisenker Is Not Limited To Pre-Metallization Passivation

Lisenker is not limited to annealing in, or passivation with, deuterium prior to formation of the metal contacts. Rather, it "can be implemented throughout the VLSI fabrication procedure." Ex. 1006, 8, ll. 29-30. The University characterizes this as an "isolated passage from Lisenker." PO

Resp. 12. But, it is not. Lisenker includes numerous additional teachings that undermine the University's argument that Lisenker's use of deuterium is limited to pre-metallization passivation, including the following:

> "In general, any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material." Ex. 1006, 4, ll. 32-34.
>
> "In one aspect of the present invention, VLSI fabrication flows employ deuterium contained compounds in many or all of the fabrication steps that would normally employ hydrogen or a hydrogen containing compound." *Id.* at 5, ll. 6-9.
>
> "The formation of Si-D and Si-OD bonds is accomplished in the present invention by contacting a silicon wafer with deuterium or a deuterium containing compound before, during, and/or after formation a device oxide layer." *Id.* at 6, ll. 10-14.
>
> "A typical fabrication procedure will include various doping, etching, annealing, deposition, cleaning, passivation, and oxidation steps. In each instance in which hydrogen or a hydrogen containing compound is employed, deuterium or a deuterium containing compound can be used in its place." *Id.* at 8, ll. 30-35.

The University, citing a 1995 publication, previously conceded that "post metal hydrogen annealing had been in widespread use in the semiconductor industry for many years[.]" Ex. 1013 ¶ 15; *see also* Ex. 1001 ¶ 15 (Micron's witness Dr. Reed testifying that it was "standard practice" in the industry). Thus, as Lisenker teaches the substitution of deuterium "[i]n each instance" in which hydrogen is otherwise used, and "throughout the VLSI fabrication procedure," it teaches that substitution during post-metal annealing. Ex. 1006, 8, ll. 29-37.

To support its argument that Lisenker is limited to pre-metallization passivation, the University cites the following deposition testimony of Micron witness Dr. Reed, taken during his cross-examination:

> Q. So Lisenker is teaching that one should not anneal the deuterium until after metallization?
>
> MR. RIFFE: Objection, form.
>
> THE WITNESS: That's not the way I read this.

PO Resp. 13 (citing Ex. 2013, 88, ll. 13-17). This testimony does not support the University's argument. As is evident on its face, counsel for the University asked Dr. Reed whether Lisenker was *limited* to post-metallization passivation, and he answered in the negative. That answer is consistent with the disclosure of Lisenker. *See, e.g.*, Ex. 1006, 8, ll. 29-30 ("The present invention can be implemented throughout the VLSI fabrication procedure.").

c) Lisenker Teaches The Claimed "substantially reduc[ing] degradation of said device associated with hot carrier stress"

The University argues that this limitation is not met in Lisenker because it lacks deuterium at the interface. PO Resp. 11-12. More specifically, the University argues that Lisenker is limited to deuterium passivation that is performed only pre-metallization (i.e., before the metal contacts on the device are formed) and, thus, the deposited deuterium migrates away from the interface during subsequent processing. *Id.* As discussed above, however, Lisenker is not limited to pre-metallization deuterium passivation.

Contrary to the University's assertions, Lisenker expressly states that deuterium is retained at the interface.

> The regions where the deuterated bonds provide the greatest benefit in terms of device performance is at the interface of silicon-silicon dioxide layers. Thus, the semiconductor devices of this invention will have at this interface a ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds that is substantially greater than ratio of naturally occurring deuterium to hydrogen.

Ex. 1006, 10, ll. 29-35. Lisenker also includes claims to such devices, including, for example, a semi-conductor device having an interface between a silicon dioxide layer and a silicon surface "wherein the ratio of Si-OD plus Si-D bonds to Si-OH plus Si-H bonds is greater than about 99:1." *Id.* at 12, ll. 3-9 and 15-17.

Thus, Lisenker teaches devices having increased amounts of deuterium at the interface relative to other prior art devices. It is inherent that the increased deuterium at the interface substantially reduces degradation associated with hot carrier stress. The University does not dispute that fact, and, indeed, it is the basis of the claims of its patent. PO Resp. 2; *see also King Pharms., Inc. v. Eon Labs, Inc.*, 616 F.3d 1267, 1276 (Fed. Cir. 2010) ("Because the '128 patent discloses no more than taking metaxalone with food, to the extent such a method increases the bioavailability of metaxalone, the identical prior art method does as well."). Additionally, Lisenker expressly recognizes the improvement. Ex. 1006, 5, ll. 4-5 ("Therefore, the deuterium containing devices of the present invention have improved stability, quality, and reliability.").

2. Claim 2

Independent claim 2 requires:

> annealing the device in an ambient including deuterium at a temperature above about 200° C. and below a decomposition or melting temperature of said structure to form a concentration of deuterium at said interface region *effective to substantially reduce degradation of said device associated with hot carrier stress by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.*

(emphasis added).

Lisenker discloses conducting the deuterium annealing preferably at about 500° C. Ex. 1006, 9, l. 20. This is within the claimed temperature range, which we have construed to include from about 200° C. to at least about 1,000° C.

The italicized portion of the above-quoted limitation is the inherent result of the claimed process, which process also is taught by Lisenker. *See King Pharms.*, 616 F.3d at 1276.

3. Claim 3

Claim 3 depends from claim 2 and additionally recites "wherein said temperature is about 400° C." Lisenker discloses conducting the deuterium annealing "preferably" at about 500° C but notes that other acceptable conditions would be apparent to a person of skill in the art. Ex. 1006, 9, ll. 20-25. Dr. Reed testified that post-metal anneals are generally conducted at about 400° C. to about 500° C. Ex. 1001 ¶¶ 15-16.

4. Claim 4

Claim 4 depends from claim 1 and additionally recites "wherein said deuterium-enriched ambient comprises deuterium gas and one or more inert gases." Lisenker discloses this additional limitation with nitrogen used as the inert gas. Ex. 1006, 8, l. 37 – 9, l. 1.

5. Claim 5

Claim 5 depends from claim 4 and additionally recites "wherein said ambient includes 1% to 100% by volume deuterium gas." Lisenker discloses this additional limitation with specific examples of 50% deuterium and "pure" (100%) deuterium. Ex. 1006, 6, ll. 16-22.

6. Claim 6

Claim 6 depends from claim 1 and additionally recites that the "ambient comprises deuterium gas and one or more of hydrogen, nitrogen, argon, and helium gas." Lisenker discloses this additional limitation wherein the ambient is a mixture of deuterium gas (D_2) and nitrogen gas (N_2). Ex. 1006, 8, l. 37 – 9, l. 1.

7. Claim 7

Claim 7 depends from claim 1 and additionally recites "wherein said insulative layer comprises an oxide or nitride of silicon." Lisenker discloses this additional limitation wherein the insulative layer is silicon dioxide. Ex. 1006, 4, ll. 20-27.

8. Claim 8

Claim 8 depends from claim 1 and additionally recites "annealing said device at a temperature of at least about 400° C." Lisenker discloses this additional limitation wherein the temperature is about 500° C. Ex. 1006, 9, l. 21.

D. Claims 1-8 As Obvious Over Lisenker In View Of Ito

Micron relies on Ito as providing an express teaching of the thickness limitations required by independent claims 1 and 2. Pet. 21. Dr. Reed testified that, at the time of filing the '533 patent, it would have been apparent to a person of ordinary skill in the art to employ insulating layers as small as 30 Angstroms in Lisenker, as taught by Ito. Ex. 1001 ¶¶ 43-44. The University does not dispute that testimony but merely argues that "Ito's teachings regarding thickness do not solve for the deficiencies associated with the afore-discussed deficiencies of the Lisenker reference." PO Resp. 16.

Micron has made a prima facie case that the subject matter of claims 1-8 would have been obvious over Lisenker in view of Ito.

E. Claims 1-8 As Obvious Over Deal In View Of Lisenker

Micron asserts that Deal teaches the subject matter of claim 1 except that Deal employs hydrogen for the post-metal anneal instead of deuterium. Pet. 25-27. We agree, *see* Ex. 1009, col. 9, ll. 46-51, and we note that the University has not disputed the asserted teachings of Deal. PO Resp. 16-17.

Micron next asserts that it would have been obvious for a person of ordinary skill in the art at the time of the invention of the '533 patent to modify Deal to employ deuterium instead of hydrogen as taught by Lisenker. Dr. Reed testified:

> At the time of the priority date of the '533 patent, the benefits of substituting deuterium for hydrogen were known. As I have discussed previously, Lisenker teaches the substitution of deuterium for hydrogen and states that such a substitution results in "bonds that are less likely to break when exposed to electrical stresses," which improves device "stability, quality, and reliability." [Ex. 1006, 5, ll. 2-5.] It would have been

> apparent to incorporate the teachings of Lisenker with the '380 patent [Deal] because both references are directed to improving the quality of the Si/SiO_2 interface, which has a direct impact on the device quality. Lisenker suggests that "any hydrogen containing material used in VLSI fabrication can be replaced with corresponding deuterium containing material," [Ex. 1006, 4, ll. 32-34] which would include the '380 patent's post-metallization anneal.

Ex. 1001 ¶ 50.

In opposing this ground of unpatentability, the University merely relies on its prior arguments regarding Lisenker. PO Resp. 16-17. However, the argument that Lisenker is limited to pre-metal annealing and, thus, results in no increase in deuterium at the interface is misplaced here (in addition to being erroneous). It is Deal, and not Lisenker, that is relied on for its teaching of post-metal annealing. That teaching is undisputed. And, as Dr. Reed testified, Lisenker suggests to the person of ordinary skill in the art to modify Deal's post-metal anneal by substituting deuterium for hydrogen.

Micron has made a prima facie case that the subject matter of claims 1-8 would have been obvious over Deal in view of Lisenker.

F. Claims 1-8 As Obvious Over Deal In View Of Ito and Lisenker

Micron relies on Ito as providing an express teaching of the thickness limitations required by independent claims 1 and 2. Pet. 43. Dr. Reed testified that, at the time of filing the '533 patent, it would have been apparent to a person of ordinary skill in the art to employ in Deal (as modified by Lisenker above) insulating layers as small as 30 Angstroms, as taught by Ito. Ex. 1001 ¶¶ 47-48. In opposition, the University does not dispute that testimony but merely argues that "[f]or the reasons set forth []

above, this combination does not render the subject claims obvious." PO Resp. 17.

Micron has made a prima facie case that the subject matter of claims 1-8 would have been obvious over Deal in view of Ito and Lisenker.

G. Objective Indicia

The University argues that certain objective indicia, or secondary considerations, demonstrate non-obviousness of the claims. *See Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966) ("Such secondary considerations as commercial success, long felt but unsolved needs, failure of others, etc., might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented. As indicia of obviousness or nonobviousness, these inquiries may have relevancy."). In particular, the University argues that the claimed invention of the '533 patent yielded unexpected results and that others failed to eliminate hot carrier effects. PO Resp. 4-8.

The University's evidence of unexpected results is not persuasive because it does not compare the results of the claimed invention of the '533 patent to the closest prior art, which is Lisenker. *See* PO Resp. 4-7; *In re Baxter Travenol Labs.*, 952 F.2d 388, 392 (Fed. Cir. 1991) ("[W]hen unexpected results are used as evidence of nonobviousness, the results must be shown to be unexpected compared with the closest prior art."). Lisenker expressly discloses that "deuterium containing devices of the present invention have improved stability, quality, and reliability" relative to those containing hydrogen. Ex. 1006, 5, ll. 4-5. Thus, when properly considering Lisenker, the beneficial results of substituting deuterium for hydrogen are expected. *See In re Skoner*, 517 F.2d 947, 950 (CCPA 1975) ("Expected

beneficial results are evidence of obviousness of a claimed invention. Just as unexpected beneficial results are evidence of unobviousness.")

With respect to the alleged failure of others, the University argues that the "continued use [in the prior art] of hydrogen passivation reflects a systemic failure in the art to solve the problem faced by the inventors of the '533 patent[.]" PO Resp. 8. Thus, the University fails to account for the prior art teachings of Lisenker, which had proposed already the substitution of deuterium for hydrogen during passivation, and indeed, throughout the VLSI fabrication process.

Having considered all of the evidence, including Patent Owner's secondary considerations evidence, we conclude that the claims would have been obvious.

CONCLUSION

Petitioner, Micron, has demonstrated by a preponderance of the evidence that claims 1-8 of the '533 patent are unpatentable under 35 U.S.C. § 103: (1) as obvious over Lisenker; (2) as obvious over Lisenker in view of Ito; (3) as obvious over Deal in view of Lisenker; and (4) as obvious over Deal in view of Lisenker and Ito.

ORDER

In consideration of the foregoing, it is hereby:

ORDERED that claims 1-8 of the '533 patent are CANCELLED.

Case IPR2013-00005
Patent 6,444,533

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US006444533B1

(12) **United States Patent**
Lyding et al.

(10) **Patent No.: US 6,444,533 B1**
(45) **Date of Patent: Sep. 3, 2002**

(54) **SEMICONDUCTOR DEVICES AND METHODS FOR SAME**

(75) Inventors: **Joseph W. Lyding**; **Karl Hess**, both of Champaign, IL (US)

(73) Assignee: **Board of Trustees of the University of Illinois**, Urbana, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/518,802**

(22) Filed: **Mar. 3, 2000**

Related U.S. Application Data

(62) Division of application No. 09/020,565, filed on Jan. 16, 1998, now Pat. No. 6,147,014, which is a continuation of application No. PCT/US97/00629, filed on Jan. 16, 1997, which is a continuation of application No. 08/586,411, filed on Jan. 16, 1996, now Pat. No. 5,872,387.

(51) **Int. Cl.**[7] **H01L 21/331**; H01L 21/26

(52) **U.S. Cl.** **438/308**; 438/795; 438/910

(58) **Field of Search** 438/257–267, 438/308, 795, 910

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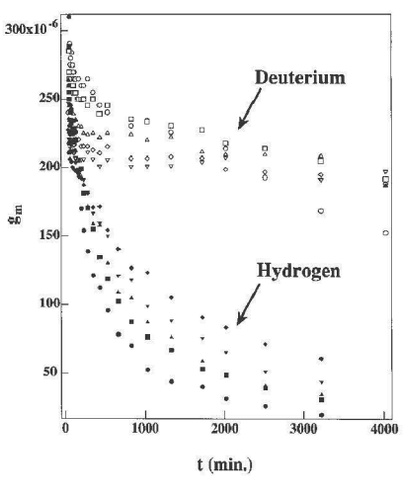
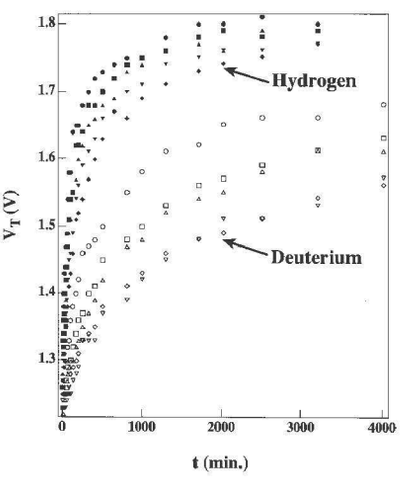
(57) **ABSTRACT**

Described are preferred processes for conditioning semiconductor devices with deuterium to improve operating characteristics and decrease depassivation which occurs during the course of device operation. Also described are semiconductor devices which can be prepared by such processes.

8 Claims, 3 Drawing Sheets





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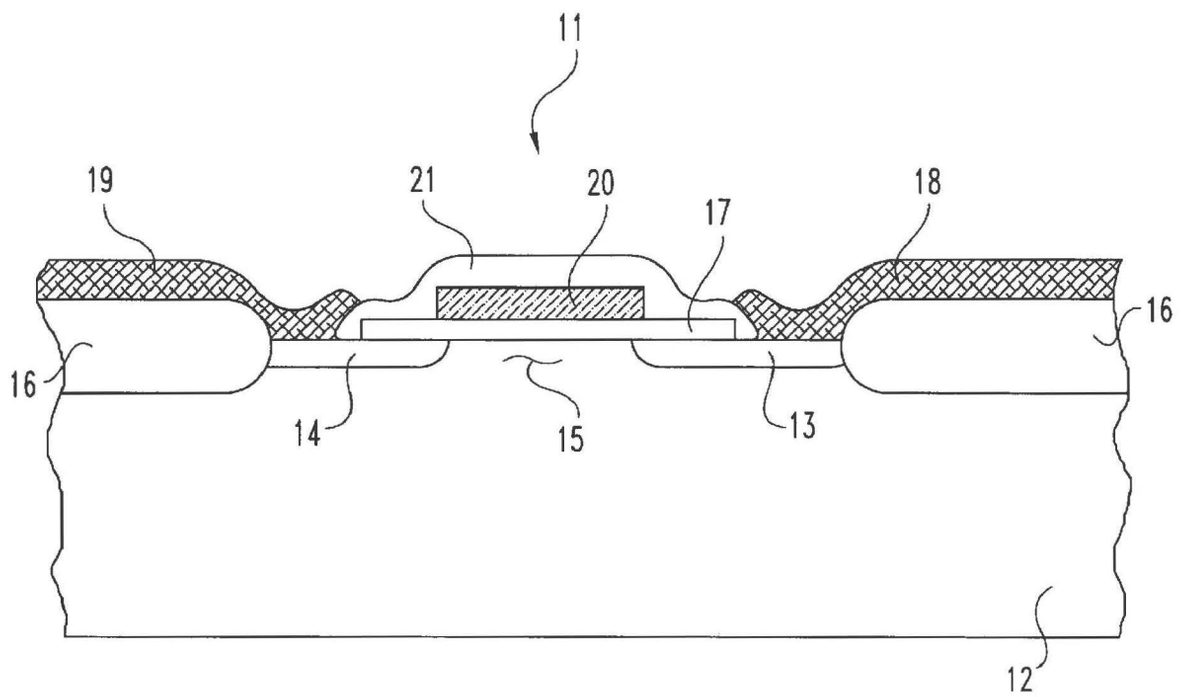


Fig. 1

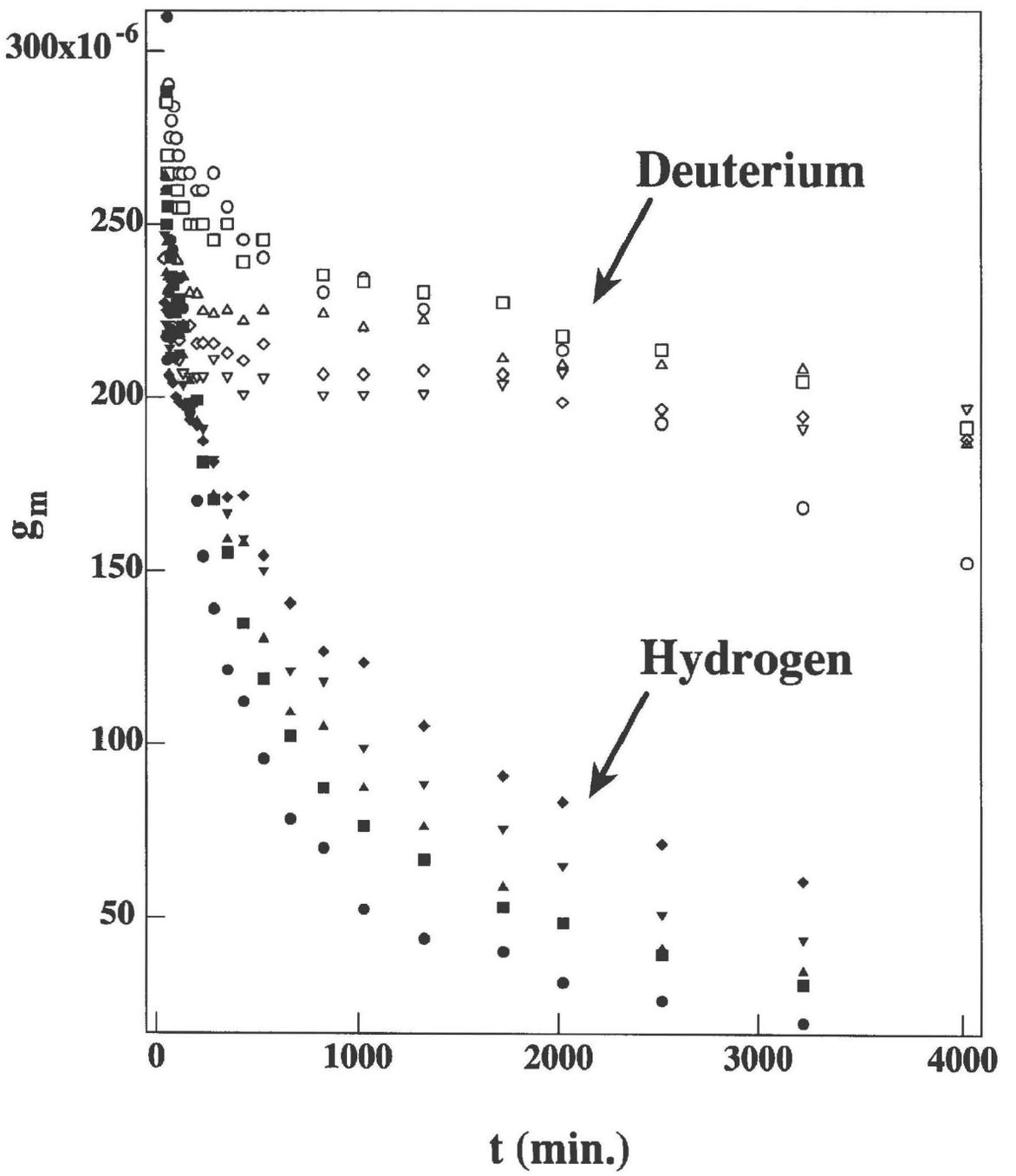

300x10-6
250
200
150
100
50
gm
Deuterium
Hydrogen
0
1000
2000
3000
4000
t (min.)

Fig. 2

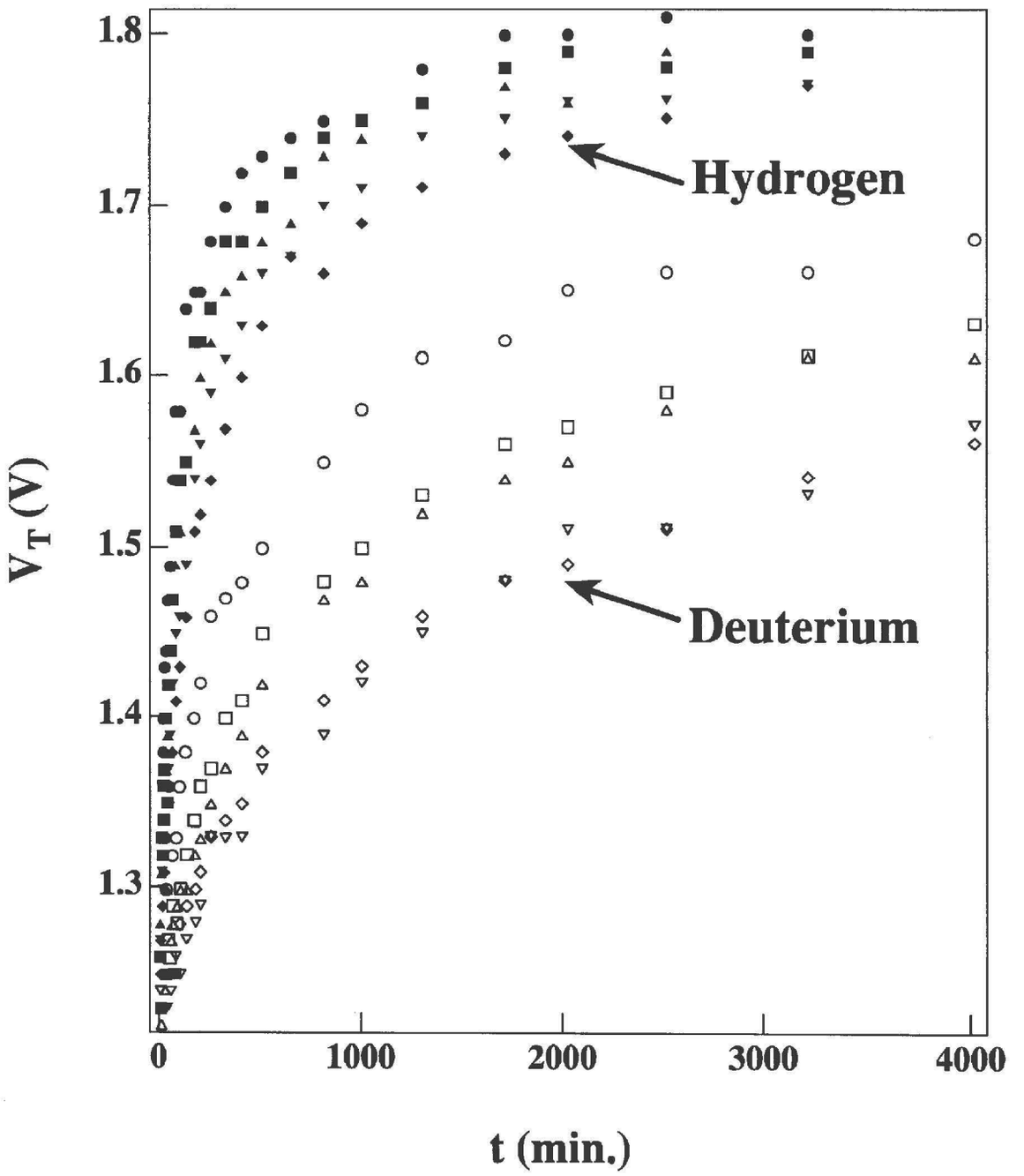

1.8
1.7
1.6
1.5
1.4
1.3
V_T (V)
Hydrogen
Deuterium
0
1000
2000
3000
4000
t (min.)

Fig. 3

SEMICONDUCTOR DEVICES AND METHODS FOR SAME

This application is a divisional of application Ser. No. 09/020,565 filed Jan. 16, 1998 (U.S. Pat. No. 6,147,014) which is a continuation of International Application PCT/US97/00629 filed Jan. 16, 1997 which is a continuation of Application 08/586,411 filed Jan. 16, 1996 (U.S. Pat. No. 5,872,387).

BACKGROUND OF THE INVENTION

The present invention resides in the field of semiconductor devices, and in particular relates to methods for treating semiconductor devices or components thereof in order to reduce the degradation of semiconductor device characteristics over time.

As further background, hydrogen passivation has become a well-known and established practice in the fabrication of semiconductor devices. In the hydrogen passivation process, defects which affect the operation of semiconductor devices are removed. For example, such defects have been described as recombination/generation centers on active components of semiconductor devices. These centers are thought to be caused by dangling bonds which introduce states in the energy gap which remove charged carriers or add unwanted charge carriers in the device, depending in part on the applied bias. While dangling bonds occur primarily at surfaces or interfaces in the device, they also are thought to occur at vacancies, micropores, dislocations, and also to be associated with impurities.

Over the years a number of hydrogen passivation processes have been proposed. For example, U.S. Pat. No. 3,923,559 describes a process in which, in the fabrication of a device such as a metal oxide semiconductor field effect transistor (MOSFET) device, hydrogen gas is introduced into the layer of silicon dioxide prior to deposition of the metal electrodes. Thereafter, the metal electrodes are deposited, thereby trapping the hydrogen gas within the device. Thereafter, the device is annealed at an elevated temperature and the hydrogen previously introduced migrates to the silicon surface to neutralize undesirable interface states produced during device fabrication.

U.S. Pat. No. 4,151,007 describes a passivation process in which the last fabrication step in the device fabrication involves heating the device in an ambient of hydrogen gas at a temperature of 650° C. to 950° C. This final hydrogen anneal step reportedly negated the effects of slow trapping and thus improved the stability of the MOS structures.

U.S. Pat. No. 4,113,514 describes a passivation process which involves exposing the device to atomic hydrogen, for example generated using a glow-discharge apparatus acting upon molecular hydrogen, at a temperature lower than 450° C. Somewhat similarly, U.S. Pat. No. 4,331,486 describes a passivation process in which a hydrogen plasma is created to treat the semiconductor devices with atomic hydrogen.

U.S. Pat. No. 3,849,204 describes a passivation process which involves implanting hydrogen ions in the area of defects, and thereafter annealing the substrate in an inert atmosphere to eliminate the interface states.

Another problem which has arisen in the semiconductor industry is the degradation of device performance by hot carrier effects. This is particularly of concern with respect to smaller devices in which proportionally larger voltages are used. When such high voltages are used, channel carriers can be sufficiently energetic to enter an insulating layer and degrade device behavior. For example, in silicon-based

P-channel MOSFETs, channel strength can be reduced by trapped energetic holes in the oxide which lead to a positive oxide charge near the drain. On the other hand, in N-channel MOSFETs, gate-to-drain shorts may be caused by electrons entering the oxide and creating interface traps and oxide wear-out. "Drain engineering" has been an emerging field attempting to cope with these problems, for example involving the use of a lightly-doped drain (LDD) in which a lightly-doped extension of the drain is created between the channel and the drain proper. For additional detail as to these and other potential measures for reducing susceptibility to hot carrier effects, reference can be made for example to U.S. Pat. Nos. 5,352,914, 5,229,311, 5,177,571, 5,098,866, 4,859,620, 4,691,433 and 4,521,698. Such solutions are, however, expensive because they typically complicate the fabrication process. Their avoidance, or at least their simplification, would be desirable.

In light of this background there exists a need for improved passivation processes and devices resulting from such processes. The present invention addresses these needs.

SUMMARY OF THE INVENTION

It has been discovered that semiconductor devices, for example including MOS devices, can be advantageously treated with deuterium to improve their operational characteristics. Accordingly, one preferred embodiment of the present invention provides a method for treating a semiconductor device which includes a step of passivating the device with deuterium. Semiconductor devices so passivated also form a part of the present invention.

In a more preferred aspect, the invention provides a semiconductor device which includes a semiconductor layer including a Group III, IV or V element, or a mixture thereof. The device also includes an insulative (dielectric) layer atop the semiconductor layer, wherein deuterium atoms are covalently bound to atoms of the Group III, IV or V element in amounts sufficient to significantly increase resilience of the device to hot carrier effects.

Additional embodiments of the invention provide processes in which deuterium-treated semiconductor devices of the invention are operated under conditions which produce hot carrier effects, and in which deuterium is introduced into the semiconductor device after fabrication is complete, and/or in one or more of a variety of fabrication steps, and the introduced deuterium is used to improve the operative characteristics of the device.

Methods and devices of the invention provide unique advantages in the field of semiconductors, their preparation and their use. For example, the provided device demonstrate improved operational characteristics and resist aging or "depassivation" due to hot-carrier effects. Moreover, devices of the invention can be operated using higher voltages to increase performance, while better resisting degradation due to hot-carrier effects. Likewise, methods of the invention are beneficial for preparing radiation hard devices, which are usually operated at higher voltages. Further, methods of the invention can be readily and economically practiced and incorporated into existing fabrication techniques, and may eliminate the need for costly and/or complicated measures otherwise taken to guard against hot electron effects, for example lightly doped drain (LDD) technology, or provide more processing flexibility in the conduct of such measure.

Additional objects, features and advantages of the invention will be apparent from the following description.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a diagram of one illustrative metal oxide semiconductor field effect transistor to which the present invention can be applied.

FIG. 2 is a graph illustrating the comparative time-dependent degradation of the transconductance for five NMOS transistors sintered in hydrogen (solid symbols) and deuterium (open symbols), as discussed in the Experimental.

FIG. 3 is a graph illustrating the comparative time-dependent increase of the threshold voltage for NMOS transistors sintered in hydrogen (solid symbols) and deuterium (open symbols), as discussed in the Experimental.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

For the purposes of promoting an understanding of the principles of the invention, reference will now be made to embodiments thereof and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, such alterations, further modifications and applications of the principles of the invention as described herein being contemplated as would normally occur to one skilled in the art to which the invention pertains.

As disclosed above, preferred embodiments of the present invention involve the use of deuterium in the fabrication of semiconductor devices and components thereof. It has been discovered that semiconductor devices can be advantageously treated with deuterium to dramatically improve their operational characteristics. For example, treatment with deuterium provides a reduction in the depassivation or "aging" of semiconductor devices due to hot-carrier effects. Such aging is evidenced, for example, by substantial degradations of threshold voltage, transconductance, or other device characteristics. In accordance with the present invention, semiconductor devices are fabricated using deuterium to condition the devices and stably reduce the extent of these degradations. This can be accomplished, for instance, by disposing molecular (D_2), atomic (°D) or ionic (D^+) deuterium in the areas of the device in which protection against hot carrier effects is desired, and causing the deuterium to covalently bond with atoms in the area so as to be stably incorporated, for example bonding to atoms of a semiconductor layer. This covalent bonding can conveniently be achieved by heating. In these regards, the particular modes by which the deuterium is provided to the desired area, e.g. by diffusion of molecular (gaseous) deuterium or implantation of atomic or ionic deuterium, and is caused to be covalently bonded in the desired area, are not critical to the broad aspects of the present invention.

Similarly, the present invention is applicable to a broad range of semiconductor devices and their fabrication processes. Generally speaking the semiconductor devices will include at least one active component therein, for example a diode, transistor, thyristor or the like. Illustrative examples include MOS-based devices such as MOSFET devices, including CMOS and NMOS technology, light-emitting diodes, laser diodes, and the like. In this regard, the MOS-based technology discussed herein is intended to encompass the use of gate conductors other than metals as is commonly practiced, and thus reference to MOS-based devices encompasses other insulated gate technologies (e.g. IGFETs). While aspects of the present invention will now be described in more detail with reference to MOSFETs (i.e. IGFETs), it will be understood that the invention is applicable to the above-mentioned and other semiconductor devices which are susceptible to aging due to hot-carrier effects and generally the effects of energetic charge carriers.

Referring now to FIG. 1, shown is a diagram of an illustrative MOSFET to which the present invention can be applied. The device 11 includes a semiconductive substrate 12, for example comprising one or more members selected from Group III, IV or V of the periodic table. The semiconductive substrate can be a p- or n-type substrate and can, for instance, be doped or undoped crystalline silicon or amorphous silicon, gallium arsenide, or gallium aluminum arsenide. The device 11 also includes a drain 13 (n- or p-type, depending on the type of substrate) and a source 14 (similarly n- or p-type) formed in the substrate 12, and a channel 15 extending therebetween. A field oxide or other electrically insulative (dielectric) layer 16 is also provided, as is a gate insulator (dielectric) 17. Insulators 16 and 17 can be formed of a single layer or of multiple layers, and can include for instance an oxide and/or nitride of silicon, e.g. a silicon dioxide, silicon nitride, silicon oxy nitride, or silicon-rich oxide film. Device 11 also includes conductive contacts 18, 19 and 20 for the drain 13, source 14 and gate insulator 17, which can include one or more conductive materials such as metals, e.g. aluminum, gold, or copper; metal suicides such as tungsten, molybdenum, tantalum or titanium silicide, or combinations thereof; polysilicon; and titanium nitride. These and other electrically conductive materials are known in the art and can be used in the present invention. The illustrated device is typical of a MOSFET employing a polysilicon gate contact, and includes an insulator 21 over the gate contact 20. The general fabrication techniques for semiconductor devices of the invention can be conventional, including conventional growth or deposition of various layers and doping operations employing appropriate masks, encapsulation, packaging and other steps.

In accordance with the invention, the semiconductor device will be treated with deuterium during or after completion of fabrication so as to condition the device to improve its operating characteristics. In the case of MOSFET devices, such improvement is thought to occur due to the elimination of interface states between the semiconductor substrate 12 (e.g. silicon) and the gate insulator 17 (e.g. silicon dioxide) by covalent bonding of deuterium atoms at the interface. Therefore, in preferred aspects of the present invention, during or subsequent to the fabrication of device 11 (e.g. subsequent to fabricating the gate, source and drain contacts), deuterium, either in atomic, ionic or molecular form, is disposed at the interface of the substrate 12 and the gate insulator 17, and caused to covalently bond to atoms at the interface, for instance atoms at the surface of the semiconductor layer.

In this regard, deuterium conditioning or passivation of the device 12 can be achieved in a variety of ways. For instance, device 11 can be heated in the presence of a flowing, mixed or static deuterium-enriched ambient at one or more stages of fabrication, and/or after fabrication is completed (i.e. after the metal contacts are completed). The deuterium-enriched ambient in accordance with the invention will contain deuterium at a level above that which occurs in nature, and above that which occurs as a low-level impurity in other supplied gases (for example purified hydrogen gas which is presently used in hydrogen passivation processes for semiconductors). Generally speaking, ambients containing 0.1% up to 100% by volume deuterium gas will be employed, more preferably about 5% to 50%, and conveniently about 5% to 20%. The deuterium-enriched ambient will preferably be completely or essentially free of oxygen, but can contain one or more other gases useful in or not deleterious to the annealing procedure. For example, hydrogen gas can be used in combination with deuterium, and/or inert gases such as nitrogen, helium, argon or the like

can be present. The annealing process can be conducted at atmospheric, subatomospheric or superatmospheric pressure, preferably at a temperature of at least about 200° C. up to the melting or decomposition temperature of other components of the device, more preferably in the range of about 200° C. to about 1000° C., and most typically in the range of about 200° C. to about 800° C. In addition, once processing in the ambient is complete, the deuterium remaining in the ambient can be recovered for recycle and later use. For instance, the ambient can be combusted so as to form heavy water (D_2O), and the heavy water processed (e.g. by electrolysis or otherwise) to again from deuterium gas.

Other methods of providing deuterium at the semiconductor/gate insulator interface, or in other areas of a semiconductor device where a reduction in the degradation of device performance by hot carrier effects, may also be used without departing from the present invention. For example, atomic deuterium can be disposed at the desired location (e.g. interface) by ion or atomic deuterium implantation and annealing techniques (see e.g. U.S. Pat. Nos. 3,849,204 and 4,113,514) and/or can be trapped within layers of the semiconductor device during fabrication and thereafter caused to migrate to the interface (see e.g. U.S. Pat. No. 3,923,559). Moreover, during the initial stages of fabrication, the surface of the semiconductive substrate **12** can be conditioned to contain covalently bonded deuterium, for example by etching with a deuterium halide such as deuterium bromide, chloride or fluoride or by treatment with a deuterium plasma. The substitution of such treatments for those currently practiced, for instance hydrogen fluoride or bromide etching or hydrogen plasma treatment, will be well within the purview of those practiced in the field of semiconductor device fabrication. Such treatment will desirably result in deuterium atoms being covalently bonded to the surface atoms of the material from which the semiconductor is constructed (e.g. a Group III, IV or V element or mixture thereof), for example being directly bonded to atoms of such material (e.g. in the case of a Si—D bond), or bonded to such atoms through oxygen or another atom (e.g. in the case of an Si—O—D covalent bonding). Thus, in the case of a silicon semiconductor, such surface treatment processes will desirably populate the surface of the semiconductor with deuterium-silicon (D—Si) and/or deuterium-oxygen-silicon (D—O—Si) bonds. The treated semiconductor material can then be used to fabricate a semiconductor device.

Additional treatments which involve the substitution of a deuterium-containing compound for a hydrogen-containing compound in device fabrication include, for instance, the use of deuterated compounds in the formation of silicon nitride (Si_3N_4) spacers which act as diffusion barriers. Conventionally, ammonia (NH_3) is reacted with an appropriate silane compound such as silane (SiH_4), disilane (Si_2H_6), or dichlorosilane ($SiCl_2H_2$) to manufacture such silicon nitride spacers. In specific aspects of the present invention, silicon nitride spacers can be manufactured from corresponding chemicals in which one or more of the hydrogens, and preferably all of the hydrogens, are replaced by deuterium. Thus, a silicon nitride spacer can be formed by reacting a compound having the formula $ND_{(n)}H_{(3-n)}$ wherein n is 1, 2 or 3, with an appropriate silane compound, e.g. $SiD_{(m)}H_{(4-m)}$ wherein m is 1, 2, 3 or 4, or $Si_2D_oH_pX_q$ wherein o is 1, 2, 3, 4, 5 or 6, p is 0, 1, 2, 3, 4 or 5, q is 0, 1, 2, 3, 4 or 5, and X is halogen such as bromo- or chloro-, with the proviso that o+p+q=6. Among these, it will be preferred to react ND_3 with SiD_4 and/or $SiCl_2D_2$ to form the silicon nitride spacer. Constructing the nitride spacer in this fashion will leave a deuterium-containing background, which will provide a deuterium source in the device which is released, e.g. during heat treatment, to passivate the oxide/silicon interface in MOS transistors or other similar devices. Appropriate chemicals for these purposes may be obtained commercially and/or manufactured using techniques generally known to the art. For instance, deuterated ammonia (ND_3) is available commercially from Isotech, Inc. of Miamisburg, Ohio. Deuterated silane (ND_4) can be prepared by reacting tetrachlorosilane ($SiCl_4$) with lithium aluminum deuteride ($LiAlD_4$) to form the deuterated silane (see, e.g. *Journal of Organometallic Chemistry*, Vol. 18, p. 371 (1969); and *Inorganic Synthesis, Vol.* 11, pp. 170–181 (1968)). Lithium aluminum deuteride for such reactions can be prepared using known procedures or can be obtained commercially from Isotech, Inc. Dideuterodichlorosilane (D_2SiCl_2) may be prepared by reacting silicon metal (Si) with deuterium chloride (DCl) to form deuterotrichlorosilane ($DSiCl_3$), which can in turn be reacted in the presence of a catalyst to form dideuterodichlorosilane (see, e.g., *Ind. Eng. Chem. Res.* 27(9), 1600–1606 (1988). These and other appropriate chemistries for preparing deuterated compounds will be readily apparent to the skilled artisan.

Still other fabrication steps which conventionally employ hydrogen-containing chemicals, and for which corresponding deuterium-containing chemicals can be used, include the growth of oxides using DCl instead of HCl to remove metal impurities, the growth of oxynitrides with deuterated ammonia, e.g. ND_3, instead of NH_3, the manufacture of polysilicon gates made with a deuterated silane or related compounds, the manufacture of epitaxial silicon layers made with deuterated silane or related compounds, wet oxidation processes using D_2O in place of H_2O, and the use of deuterated dopants such as AsD_3, PD_3, B_2D_6, or the like. These and other similar processes can be used to provide a deuterium-containing background in the device, which will release deuterium to condition the semiconductor device.

Techniques described herein other than annealing in a gaseous deuterium ambient, e.g. those which involve ion implantation and/or entrapment of deuterium during fabrication for later migration and passivation, can effectively facilitate passivation where structures are contained in the device which hinder the passage of deuterium gas to the interface of the semiconductor and insulative layer. For example, the presence of silicon nitride layers above the interface hinders the diffusion of deuterium gas to the interface, and thus the use of alternate or additional methods of providing deuterium to the interface, as described above, can optionally be used to facilitate device passivation.

The conditioning of the semiconductor device with deuterium has been found to significantly reduce effects associated with depassivation of the device by hot-carrier (e.g. hot-electron) effects. For example, as reported in the Experimental below, dramatic decreases in the degradation of threshold voltage and transconductance are observed when deuterium is used to passivate the devices, as compared to hydrogen passivation (see FIGS. **2** and **3**, respectively). These decreases represent practical lifetime improvements by factors of about ten to fifty, and also make possible the operation of the semiconductor devices at higher voltages while better resisting aging due to hot electron effects.

In order to promote a further understanding and appreciation of the present invention and its advantages, the following experimental is provided. It will be understood that this experimental is illustrative, and not limiting, of the invention.

EXPERIMENTAL

1. MATERIALS AND EQUIPMENT

1.1 Wafers

The wafers used in these examples contained NMOS transistor structures fabricated using AT&T's 0.5 μm 3.3 volt CMOS technology generally as described in I. C. Kizilyalli and M. J. Thoma, et al., IEEE Trans. Semiconductor Manufacturing 8, 440 (1995), with the following changes. The gate oxide was reduced to t_{ox}~55 Å, the doping in the p-well was increased, and the phosphorous-doped LDD region was replaced by a shallow arsenic implanted (dose=4×10^{14} cm^{-2} at 30 keV) source-drain extension region. With these modifications, the peak value for the source-drain peak electric field near the drain edge of the gate is enhanced, resulting in more channel hot electrons. The shallow source-drain extension insures that these hot electrons are near the Si/SiO_2 interface, where they will cause significant interface damage. The interface damage, caused by these hot carriers, can easily by observed by monitoring the changes in NMOS transistor transconductance (i.e. $g_m=\Delta I_{DS}/\Delta V_{GS}|V_{DS}$) or by the shift in transistor threshold voltage V_{th}. See, J. M. Pembley et al in Advanced CMOS Process Technology, VLSI Electronics Microstructure Science, Vol. 19, Academic Press: San Diego, 1989.

1.2 Gases

Hydrogen, nitrogen and deuterium gases were obtained from S. J. Smith Welding Supply, Decatur, Ill., U.S.A. All gases were ultra high purity (UHP), 99.999% pure. The source of the deuterium gas was MG Industries of Morrisville, Pa., U.S.A.

1.3 Furnace Set-Up

Wafers were annealed using a two-zone Marshall muffle furnace set up for feed of nitrogen and either hydrogen or deuterium through the zones. Wafers were positioned on a sliding quartz tray and positioned with a quartz pushrod. Both zones of the furnace were set to the desired annealing temperature and then the rheostats of the wafer annealing zones were adjusted to achieve substantially constant temperature: across the holding area of the quartz tray. This tray was positioned the same for each run. Temperatures were measured using a type K thermocouple fed into the furnace through an O-ring sealed stainless steel feedthrough on the furnace tube insert end caps. Another type K thermocouple was placed in an ice bath (deionized water) to serve as the zero 0° C. reference. The temperature between the two thermocouples was measured using a PROTEK TM BOOK battery operated thermocouple meter. The furnace zones were connected to two Barber Coleman 570 temperature controllers which used the fixed thermocouples (10.5 inches from the furnace ends) for feedback. For gas flow, the ends of the furnace quartz tube insert were tapered ground glass joints for which mating glass end caps were fashioned. Because the ends of the tubes were well outside of the furnace, they were not hot and a gas tight seal could easily be formed using Teflon tape. A cylinder containing the hydrogen or deuterium was connected to the furnace gas tube with a Matheson Model 3122-350 two stage regulator with a metal diaphragm to preserve gas purity. The gases were plumbed to the quartz tube end cap by means of 304 stainless steel tubing. The nitrogen gas line was interfaced to the glass end cap by means of an O-ring sealed stainless steel quick connector. The hydrogen and deuterium gas lines shared a similar connector, with only one of these gases being connected at any given time to avoid the possibility of cross-contamination between the hydrogen and deuterium lines. As a further precaution, the deuterium gas line contained a series coil of copper tubing which was immersed in liquid nitrogen to remove any moisture that might otherwise introduce hydrogen into the furnace. During the anneal runs, the gas flowed through the zone of the furnace which did not contain the wafer samples before entering the wafer zone. In this manner, the gas was preheated, thereby not perturbing the wafer zone temperature. After exiting the wafer zone, the gas flowed out through a fitting on the opposite end cap and was then routed through a Matheson P6-1000 series flowmeter (0.1 through 2.0 standard liters per minute (SLPM) range). After the flowmeter, the gas was exhausted through a standard hood vent.

2. ANNEALING RUNS

In all runs, nitrogen gas flow was set at 0.55 SLPM. To achieve an ambient containing about 10% by volume hydrogen or deuterium gas, the pressure was increased to about 0.61 SLPM by opening the hydrogen or deuterium gas regulator. In a first run, wafer samples were annealed in an ambient of 10% deuterium in nitrogen for a period of about 1 hour. The temperature was maintained at about 400° C. In a second run, wafer samples were annealed in a 10% by volume hydrogen in nitrogen ambient for a period of about 1 hour at a temperature of about 400° C. Devices on the resulting wafers were subjected to electrical stress testing. In particular, accelerated hot carrier DC stress experiments were performed on transistors with varying gate lengths (0.5 μm to 15 μm) at peak substrate current conditions. The applied stress voltages were V_{DS}=5V and V_{GS}~2V. Pre-stress transistor measurements demonstrate that devices sintered in hydrogen and deuterium have identical electrical characteristics (e.g. transconductance, threshold voltage, substhreshold-slope, saturation current, and the like).

FIG. **2** shows the transconductance degradation as a function of stress time for NMOS transistors with five gate lengths ranging from 0.5 to 0.7 μm. In FIG. **3** the threshold voltage increase as a function of stress time is shown for the same devices. As can been seen, wafers sintered in a deuterium ambient exhibit dramatically higher levels of resilience to channel hot carrier stress. In further comparative study, about 80 additional transistors were similarly stressed, and the same strong trend was observed. These results show that if 20% transconductance degradation is taken as a practical lifetime criteria, transistors sintered in deuterium typically exhibit lifetimes 10 times longer than those sintered in hydrogen. A factor of 10 improvement in lifetime is also inferred if a shift of 100 mV (or 200 mV) in threshold voltage is taken as the degradation criteria.

While the invention has been illustrated and described in detail in the foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only the preferred embodiments have been described and that all changes and modification that come within the spirit of the invention are desired to be protected. In addition, all publications cited herein are indicative of the level of skill in the art and are hereby incorporated by reference as if each had been individually incorporated by reference and fully set forth.

What is claimed is:

1. A process for treating a semiconductor device including a semiconductor region and an insulating layer having an interface with the semiconductor region and a contact on said insulating layer overlying said interface, comprising the steps of forming said insulating layer with a thickness not exceeding about 55 Angstroms beneath said contact, and of annealing said semiconductor device, subsequent to completion of fabrication of said device, in an ambient including deuterium to form a concentration of deuterium at the

interface between said semiconductor region and said insulating layer region effective to substantially reduce degradation of said device associated with hot carrier stress.

2. A process for treating an insulated gate field effect transistor device structure including a channel region extending between source and drain regions, a gate insulating layer having an interface with said channel region, and contacts to said source and drain regions and on said gate insulator layer, comprising forming said gate insulator beneath the gate contact to have a thickness not greater than about 55 Angstroms and, subsequent to formation of said source, drain and gate contacts, annealing the device in an ambient including deuterium at a temperature above about 200° C. and below a decomposition or melting temperature of said structure to form a concentration of deuterium at said interface region effective to substantially reduce degradation of said device associated with hot carrier stress by increasing a practical lifetime at least about 10 times that provided by a corresponding passivation with hydrogen, where practical lifetime is taken as 20% transconductance degradation as a result of electrical stress.

3. A process according to claim **2**, wherein said temperature is about 400° C.

4. The method of claim **1** wherein said deuterium-enriched ambient comprises deuterium gas and one or more inert gases.

5. The method of claim **4** wherein said ambient includes 1% to 100% by volume deuterium gas.

6. The method of claim **1** wherein said ambient comprises deuterium gas and one or more of hydrogen, nitrogen, argon, and helium gas.

7. The method of claim **1** wherein said insulative layer comprises an oxide or nitride of silicon.

8. The method of claim **1**, which comprises annealing said device at a temperature of at least about 400° C.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,444,533 B1
DATED : September 3, 2002
INVENTOR(S) : Joseph W. Lyding et al.

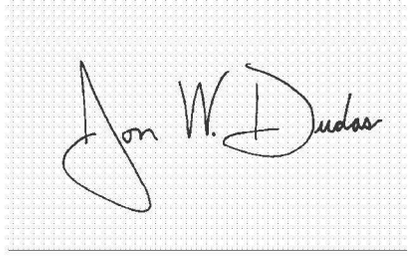
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,
Line 4, immediately after the title, please insert the following new paragraph:

-- GOVERNMENT RIGHTS
This invention was made with government support under Grant No. N00014-92-J-1519 awarded by the Department of Navy Research. The government has certain rights in the invention. --

Signed and Sealed this

Third Day of August, 2004



JON W. DUDAS
Acting Director of the United States Patent and Trademark Office

CERTIFICATE OF SERVICE

I hereby certify that on the 29th day of July, 2014, I electronically filed the foregoing BRIEF OF APPELLANT THE BOARD OF TRUSTEES OF THE UNIVERSITY OF ILLINOIS using the CM/ECF system of the Court, which will send a notice of electronic filing to the following counsel of record:

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Appellant will hand deliver six paper copies of this document, as filed with the CM/ECF system of the Court, to the Clerk of the Court of Appeals for the Federal Circuit in Washington D.C. pursuant to ECF-10(B).

/s/ George C. Summerfield
George C. Summerfield

CERTIFICATE OF COMPLIANCE

Pursuant to Fed. R. App. P. 32(a)(7)(C), the undersigned hereby certifies that this brief complies with the type-volume limitation of Fed. R. App. P. 32(a)(7)(B)(i).

1. Exclusive of the exempted portions of the brief, as provided in Fed. R. App. P. 32(a)(7)(B), the brief contains 2,103 words.

2. The brief has been prepared in proportionally spaced typeface using Microsoft Word in 14 point Times New Roman font. As permitted by Fed. R. App. P. 32(a)(7)(B), the undersigned has relied upon the word count feature of this word processing system in preparing this certificate.

July 29, 2014

/s/ George C. Summerfield
George C. Summerfield